REMARKS

Claims 1-51 are pending in the present application. Claims 1, 23, 34, 41, 45-47, and 49-51 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 32, 33 and 46 stand objected to for informalities stated in the Office Action. The claims are amended above in a manner consistent with suggestions provided in the Office Action. Claim 32 is amended to remove the strike-through phrase "buffered". With regard to the objection to claim 46, the Applicant notes that in the examples provided in the present specification at FIGs. 6 and 7, a "second read clock signal", for example signal RCLK_OUT, is generated "in response to and in phase with" a "first read clock signal", for example signal RCLK_IN. It is therefore requested that examination of claim 46 be carried out in view of the literal wording of the claim as stated. Removal of the objections is respectfully requested.

Claims 1-4, 6-11, 26, 27, 29, 31-42, 44-47, 50 and 51 are rejected as being unpatentable over Halbert, *et al.* (U.S. Patent No. 6,625,687) in view of Gustavson (U.S. Patent No. 6,442,644), Dodd (U.S. Patent No. 6,530,006), Hansen (U.S. Patent No. 5,742,840) and the Applicant's admitted prior art (AAPA). Claims 5 and 28 are rejected as being unpatentable over Halbert, *et al.* in view of Gustavson, Dodd , Hansen, AAPA, and Johnson, *et al.* (U.S. Patent No. 5,987,576). Claims 23 and 49 are rejected as being unpatentable over Halbert, *et al.* in view of Dodd. Claims 24, 25, 30 and 43 are rejected as being unpatentable over Halbert, *et al.* in view of Dodd, Hansen and AAPA. Reconsideration and removal of the rejections are respectfully requested.

Independent claims 1 and 45-47 are amended above to state that the "the first read clock signal and the second write clock signal" are "transmitted over independent signal lines".

Independent claims 23, 34, 49 and 50 are amended above to state that "the memory module" generates "a second write clock signal for timing the transmission of data in the first

direction of transmission on the second data bus" and that " the first read clock signal and the second write clock signal" are "transmitted over independent signal lines".

Independent claims 41 and 51 are amended above to state that "the first write clock signal and the second read clock signal are transmitted over independent signal lines".

With regard to claims 1, 23, 34, 45-47, 49 and 50, the "first read clock signal" and the "second write clock signal" are transmitted over "independent signal lines", and thus are two distinct clock signals that propagate in different first and second directions of transmission on separate lines, rather than sharing a common signal line. With regard to claims 41 and 51, "the first write clock signal and the second read clock signal are transmitted over independent signal lines", and are thus two distinct clock signals on separate lines.

Halbert is related to a memory system that includes a plurality of memory modules in a daisy chain configuration and the daisy-chained memory modules are connected in a ring configuration with the memory controller. A memory bus 550 includes a plurality of lines that may include data lines, addressing lines, command lines, and clock lines (see Halbert, column 6, lines 11-16).

Gustavson is related to a memory system that has synchronous-link DRAM (SLDRAM) devices and a controller. During a read operation, the clock signals DCLK0 and DCLK1 for timing the transmission of data on the DQ_A bus are originated at one of the SLDRAM modules (110-118) that has control over the DQ_A bus 155a at that time. During write operations, the clock signals DCLK0 and DCLK1 are originated by the command module 150 which has control over the DQ_A bus 155a. The clocks for both the read and write operations are thus transmitted over the same lines. (See Gustavson, FIG. 1A, and the corresponding discussion at column 9, line 20 - column 10, line 26).

Dodd is related to a clock circuit that is embedded in an address/command buffer. The clock circuit receives an input clock and generates an output clock to the data buffers and/or the memory devices in an effort to control clock-skew (see Dodd, FIG. 3).

It is respectfully submitted that the cited references, whether alone, or in combination, fail to teach or suggest the present invention as claimed. In particular, the references fail to teach or suggest the feature of the "first read clock signal" and the "second write clock signal" being transmitted over "independent signal lines" as claimed in claims 1, 23, 34, 45-47, 49 and 50, and further fail to teach or suggest "the first write clock signal and the second read clock signal" being "transmitted over independent signal lines" as claimed in claims 41 and 51. None of the references teach or suggest generating a write clock signal in a first direction of transmission and a read clock signal in a second direction of transmission that are transmitted over independent signal lines, as claimed.

Accordingly, reconsideration of the rejections and allowance of independent claims 1, 23, 34, 41, 45-47, and 49-51 are respectfully requested. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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